AMENDMENTS TO THE CLAIMS

Claims 1-6 (canceled):

Claim 7 (previously presented): An active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection; and

a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said main memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements, said circuit comprising

> a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory, each of said plurality of circuits comprising:
>
> > a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to its associated respective one of

said plurality of processing elements; and wherein each of said plurality of logic circuits comprises:

a first input, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory;

an output;

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

Claim 8 (original): The active memory device according to claim 7, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claim 9 (previously presented): An active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection; and

a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said main memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements, said circuit comprising

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory, each of said plurality of circuits comprising:

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to its associated respective one of

said plurality of processing elements; and wherein each of said plurality of logic circuits each comprises:

a first input, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory;

an output;

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

Claim 10 (original): The active memory device according to claim 9, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claims 11-13 (canceled):

Claim 14 (previously presented): An active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits comprising:

a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory, and an output coupled to said single bit input of a respective one of said plurality of processing elements,

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to said output of said data path circuit; and wherein each of said plurality of logic circuits comprises:

a first input, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit;

an output;

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer; and

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

Claim 15 (original): The memory device according to claim 14, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claim 16 (previously presented): An active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits comprising:

a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory, and an output coupled to said single bit input of a respective one of said plurality of processing elements;

a first multiplexer having a plurality of first multiplexer inputs, each of said plurality of first multiplexer inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to said output of said data path circuit; and wherein each of said plurality of logic circuits comprises:

a first input, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit;

an output;

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer; and

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

Claim 17 (original): The active memory device according to claim 16, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claim 18 (canceled)

Claim 19 (original): The circuit according to claim 20, wherein said output of said second tri-sate device is coupled to a different data bus than said output of said first tri-state device.

Claim 20 (original): A circuit for connecting a memory device and a processing element of an active memory comprising:

a first multiplexer having a first input coupled to said processing element and a second input coupled to a data bus of said memory device;

a first register having an input and an output, said input being coupled to an output of said first multiplexer;

a second multiplexer having an input coupled to said output of said first register and an output coupled to said processing element;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said data bus;

a second tri-state device having an input coupled to said output of said first register and an output coupled to said data bus and a third input of said first multiplexer;

a second register having an input coupled to said output of said first multiplexer;

a third multiplexer having a first input, a second input, and an output, said first input being connected to an output of said second register, said output from said first register being coupled to said second input, said output being coupled to said input of said second multiplexer; and

a fourth multiplexer having a first input, a second input, and an output, said first input being coupled to said output of said first register, said second input being coupled to said output of said second register, said output being coupled to said input of said first and second tri-state devices.

Claim 21 (original): The circuit according to claim 20, wherein said output of said second tri-sate device is coupled to a different data bus than said output of said first tri-state device.

Claims 22-27 (canceled):

Claim 28 (previously presented): A processing system comprising:

a processing unit; and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection; and

a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said main memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements, said circuit comprising:

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory, and each of said plurality of circuits comprising:

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to its associated respective one of said plurality of processing elements; and wherein each of said plurality of logic circuits comprises:

a first input, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory;

an output;

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

Claim 29 (original): The processing system according to claim 28, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claim 30 (previously presented): A processing system comprising:

a processing unit; and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection; and

a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements, said circuit comprising:

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory, and each of said plurality of circuits comprising:

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to its associated respective one of said plurality of processing elements; and wherein each of said plurality of logic circuit comprises:

a first input, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory;

an output;

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

Claim 31 (original): The processing system according to claim 30, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claim 32 (original): The processing system according to claim 22, wherein said processing unit and said active memory device are on a same chip.

Claims 33-35 (canceled):

Claim 36 (previously presented): A processing system comprising:

a processing unit; and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits comprising:

a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory;

an output coupled to said single bit input of a respective one of said plurality of processing elements;

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to said output of said data path circuit; and wherein each of said plurality of logic circuits comprises:

a first input, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit;

an output;

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer; and

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

Claim 37 (previously presented): The processing system according to claim 36, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claim 38 (previously presented): A processing system comprising:

a processing unit; and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits comprising:

a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory;

an output coupled to said single bit input of a respective one of said plurality of processing elements;

a first multiplexer having a plurality of first multiplexer inputs, each of said plurality of first multiplexer inputs being coupled to an output of a respective one of a plurality of logic circuits, and an output coupled to

said output of said data path circuit; and wherein each of said logic circuit comprises:

a first input, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit;

an output;

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer;

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

Claim 39 (original): The processing system according to claim 38, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

Claims 40-51 (canceled):